Claims

What is claimed is:

1. A method of processing a memory chip, comprising:
   checking a group of memory cells on said memory chip for a defect; and
   storing in a first register a column address of any defective memory cell found during said act of checking, wherein said act of storing results in removing any other column address stored in said first register, and wherein said act of storing comprises storing said column address without a row address of said any defective memory cell.

2. The method in claim 1, wherein said act of storing comprises storing said column address in a first register located on said memory chip.

3. The method in claim 2, further comprising an act of repairing said memory chip based on data stored in said first register.

4. The method in claim 3, wherein said act of repairing comprises repairing said memory chip further based on data stored in a second register indicating redundant element availability.

5. The method in claim 4, further comprising:
   providing a signal related to blowing a programmable element associated with a column address stored in said first register;
   halting said signal before fully programming said programmable element; and
   completely programming said programmable element despite said act of halting said signal.

6. A method of repairing a memory circuit comprising a plurality of memory cells, wherein at least one memory cell of said plurality tests as defective, said method comprising:

associating redundant memory cells with each memory address incorporating a column address of a memory cell that tests as defective; and

providing said column address to circuitry on said memory circuit, wherein said circuitry is configured to carry out said act of associating, wherein said act of providing comprises providing said column address from a first register included as a part of said memory circuit, and wherein said first register is configured to store said column address to the exclusion of any other column address at the same time.

7. The method in claim 6, further comprising an act of isolating main memory cells initially related to said column address.

8. The method in claim 7, further comprising:

searching for at least one available redundant memory cell;

recording data relating to availability of said at least one redundant memory cell on a second register; and

providing said data to said circuitry.

9. The method in claim 8, wherein said act of associating redundant memory cells comprises programming at least one programmable element coupled to at least one of said redundant memory cells.

10. The method in claim 9, wherein:

said act of programming comprises transmitting an input signal to said circuitry;

said act of associating redundant memory cells comprises transmitting from said

circuitry an output signal in response to said circuitry receiving said input signal, wherein said output signal is used to program said at lease one programmable element; and

said act of transmitting an input signal comprises transmitting said input signal for a time less than that needed to program said at least one programmable element.

11. A method of preparing to repair a memory array on a die having a first redundant plane comprising at least a first redundant element and a second redundant plane comprising at least a second redundant element, said method comprising:

searching for a first available redundant element within said first redundant plane and a second available redundant element within said second redundant plane; and

storing in a first register data related to said first available redundant element and to said second available redundant element, wherein said memory array and said first register share a common substrate.

12. The method in claim 11, wherein said act of providing a first redundant plane comprises providing a first redundant plane configured to accommodate at most a first portion of memory cells of said memory array.

13. The method in claim 12, wherein said act of providing a second redundant plane comprises providing a second redundant plane configured to accommodate at most a second portion of memory cells of said memory array, said second portion being discrete from said first portion.

14. The method in claim 13, wherein said act of searching comprises searching for a column of available redundant elements, wherein said column comprises at least one cell from said first redundant plane and one cell from said second redundant plane; and

wherein said act of storing comprises storing over time data related to all available redundant columns.

15. The method in claim 14 wherein said act of storing over time comprises storing at any particular time data related to at most one available redundant column.

16. The method in claim 15, wherein said act of storing over time comprises storing data related to only the latest available redundant column found during said act searching.

17. The method in claim 16, wherein said act of storing over time comprises ultimately storing data related to only a last available redundant column found during said act of searching.

18. The method in claim 17, further comprising:

providing a third redundant plane for said memory array, wherein said third redundant plane comprises at least a third redundant element, and wherein said second redundant plane is configured to accommodate at most a third portion of memory cells of said memory array;

searching for any available redundant column at least partially within said third redundant plane; and

storing in a second register data related to an available redundant column within said third redundant plane, wherein said memory array and said second register share said common substrate.

19. A method of allowing repair of a memory array in a packaged part, wherein said memory array comprises a plurality of redundant planes, and wherein said plurality is configured to accommodate all rows of at least one column address in said memory array, wherein each plane of said plurality comprises at most a portion of at least one redundant column, said method comprising:

checking said plurality for redundant columns that remain available from any

earlier repair procedure; and

storing information relating to an available redundant column, wherein said act of storing is accomplished using a redundancy register corresponding to said plurality.

20. The method in claim 19, wherein said act of storing information comprises storing a redundant column address of said available redundant column.

21. The method in claim 20, wherein said act of storing information comprises refraining from storing a redundant row address of said available redundant column.

22. The method in claim 21, further comprising an act of programming multiple programmable elements in multiple redundant planes, wherein addresses of said multiple programmable elements are respectively stored in said plurality of redundancy registers.

23. The method in claim 22, further comprising:

providing an address register for said memory array;

checking for an error in a cell included in said memory array; and

storing information relating to said error in said address register.

24. The method in claim 23, wherein said act of providing an address register comprises providing an address register within said packaged part; and wherein said act of storing information relating to said error comprises storing a column address, to the exclusion of a row address, of a cell having said error.

25. A method of programming a programmable element, comprising:

initiating a programming signal for said programmable element using an input signal;

maintaining said programming signal for a time sufficient to program said programmable element; and

changing said input signal before said time passes.

26. The method in claim 25, wherein said act of initiating comprises initiating using said input signal and a timing signal.

27. The method in claim 25, wherein said act of initiating comprises initiating using a DQ signal.

28. A method of altering a timing signal for a circuit, comprising:

preventing said timing signal from being directly input into said circuit;

logically relating said timing signal with a delayed signal based on said timing signal; and

transmitting an output signal to said circuit, said output signal resulting from said act of logically relating.

29. The method in claim 28, wherein said act of logically relating comprises logically relating said timing signal with an inverted signal based on said timing signal.

30. The method in claim 29, wherein said act of logically relating comprises logically relating said timing signal with an inverted signal based on said delayed signal.

31. The method in claim 30, wherein said act of logically relating comprises logically relating said timing signal with said inverted signal and with an input signal configured to alter an output of said circuit.

32. A method of affecting an output of a synchronous circuit due to a change in an input signal transmitted to said circuit, comprising:

intercepting a clock signal outside of said circuit;

intercepting said input signal outside of said circuit;

transmitting said clock signal to at least one logic device;

transmitting an inverted and delayed version of said clock signal to said at least one logic device;

transmitting said input signal to said at least one logic device; and

transmitting a modified clock signal from said at least one logic device to said synchronous circuit.

33. The method in claim 32, wherein said act of transmitting a modified clock signal comprises:

performing at least one logic operation on said clock signal, said inverted and delayed version of said clock signal, and said input signal; and

as a result of said act of performing, transmitting a modified clock signal that extends a time between clock pulses in relation to that of said clock signal.

34. A method of programming at least one memory chip, comprising

transmitting a first configuration of signals to said at least one memory chip, wherein said first configuration of signals is relevant to programming a first element on said at least one memory chip, and wherein a duration of said first configuration of signals lasts for a time insufficient to program said first element; and

initiating a programming signal based on said act of transmitting a first configuration of signals, wherein a duration of said programming signal lasts for a time sufficient to program said first element.

35. The method in claim 34, further comprising:

transmitting a second configuration of signals to said at least one memory chip, wherein said act of transmitting a second configuration of signals occurs after said act of transmitting a first configuration of signals, and wherein said second configuration of signals is relevant to programming a second element on said at least one memory chip; and

maintaining said programming signal during at least a portion of said act of

transmitting a second configuration of signals.

36. The method in claim 35, wherein said act of transmitting a first configuration of signals comprises transmitting a first configuration of signals to a plurality of memory chips; and wherein said method further comprises:

programming said first element on a first memory chip of said plurality of memory chips with said programming signal; and

refraining from programming said first element on a second memory chip of said plurality of memory chips despite said programming signal.

37. The method in claim 36, wherein said act of transmitting a first configuration of signals comprises transmitting a first configuration of signals including an address signal; and wherein said act of refraining from programming comprises:

comparing data represented by said address signal with data stored in a register on said second memory chip; and

disregarding said programming signal in response to finding a lack of a match between said data represented by said address signal and said data stored in said register.

38. The method in claim 37, wherein said act of comparing data comprises comparing data represented by said address signal with a single address stored in said register.

39. The method in claim 38, wherein said act of comparing data comprises comparing data represented by said address signal with a single column address stored in said register.

40. A method of operating a plurality of redundant planes of a memory device, comprising:

identifying a memory cell of said memory device that fails a test; and

accessing at least one redundant element in each plane of said plurality of

redundant planes, wherein one redundant element of said at least one redundant element replaces said memory cell.

41. The method in claim 40, wherein said act of accessing comprises associating said at least one redundant element in said each plane with a respective memory address.

42. The method in claim 41, wherein said act of accessing comprises programming at least one programmable element.

43. The method in claim 42, wherein said act of programming comprises blowing at least one anti-fuse.

44. The method in claim 43 wherein said act of accessing comprises accessing at least one redundant element in each plane of said plurality of redundant planes, wherein every redundant element of said at least one redundant element has a common column address.

45. A timing circuit, comprising:

a first input terminal configured to receive a clock signal;

a second input terminal configured to receive a logic control signal;

an output terminal configured to transmit a modified clock signal that is slower than said clock signal;

a logic gate coupled to said output terminal, said first input terminal, and to said second input terminal;

a delay element coupled to said first input terminal; and

an inverter coupled to said logic gate.

46. The timing circuit in claim 45, wherein said inverter is coupled to said delay element.

47. The timing circuit in claim 46, wherein said inverter is coupled to said first input terminal through said delay element.

48. The timing circuit in claim 47, wherein said delay element is coupled to said logic gate through said inverter.

49. A clock circuit, comprising:

a delay element;

an inverter coupled to said delay element and configured to receive a first periodic signal; and

a logic circuit configured to transmit a second periodic signal to another circuit, wherein said second periodic signal defines a greater period that of said first periodic signal, wherein said logic circuit is coupled to said inverter and said delay element, and wherein said logic circuit is configured to receive said first periodic signal and another signal configured to alter an output of said another circuit.

50. Input circuitry for a logic circuit of a memory device, wherein said logic circuit is configured to allow access to at least one redundant memory cell of said memory device, said circuitry comprising a register on said memory device, coupled to said logic circuit, and configured to store data relevant to an available redundant memory cell.

51. The circuitry of claim 50, wherein said register is configured to store data relevant to an available redundant memory column.

52. The circuitry of claim 51, wherein said register is configured to store data relevant to every available redundant memory column found during a search for an available redundant column.

53. The circuitry of claim 52, wherein said register is sized to store data relevant to at most one available redundant memory column found during said search for an available redundant column.

54. The circuitry of claim 53, wherein said register is configured to store data relevant to at most one available redundant memory column at a time.

55. The circuitry of claim 54, wherein said register is configured to store data relevant to a last available redundant memory column found by a conclusion of said search.

56. A repair system for a memory device comprising at least one redundant plane, said system comprising a first address storage device included as a part of said memory device, wherein said first address storage device is configured to store an address associated with at least one redundant plane of said memory device.

57. The system of claim 56, wherein said first address storage device is configured to store an address associated with a first plurality of redundant planes.

58. The system of claim 57, further comprising a second address storage device configured to store an address associated with at least one redundant plane of said memory device.

59. The system of claim 58, wherein said second address storage device is configured to store an address associated with a second plurality of redundant planes, and wherein said second plurality of redundant planes is discrete from said first plurality of redundant planes.

60. A computer system, comprising:

a microprocessor;

a system clock circuit coupled to said microprocessor; and

a memory-containing device coupled to said microprocessor and comprising:

an array of primary memory cells,

an array of redundant memory cells,

a bank of programmable elements coupled to said array of primary memory cells and said array of redundant memory cells,

logic circuitry coupled to said bank of programmable elements, wherein said logic circuitry is configured to control a programming state of said programmable elements, and

a system clock modifier coupled to said logic circuitry and to said system clock.

61. The computer system of claim 60, further comprising a register coupled to said logic circuitry and sized to store at most one column address of a primary memory cell.

62. The computer system of claim 60, further comprising a register coupled to said logic circuitry and sized to store at most one column address of a redundant memory cell.

63. Redundancy circuitry for a chip, comprising:

a plurality of redundant memory cells on said chip, wherein said cells are organized into at least one redundant row, at least one redundant column, and at least two redundant planes; and

a storage device on said chip configured to store data relevant to multiple redundant planes.

64. The circuitry in claim 63, wherein said storage device is configured to store data relevant to at most one redundant column.

65. The circuitry in claim 64, wherein said storage device is configured to store data relevant to at least one redundant row.

66. The circuitry in claim 65, wherein said storage device is configured to store only a column address.

67. A storage system for a memory device on a semiconductor die, said system comprising:

a first storage device on said die and configured to store at most a partial memory address; and

a second storage device on said die and configured to store at most a partial memory address.

68. The system in claim 67, wherein said first storage device is configured to store at most a partial memory address of a main memory array of said memory device.

69. The system in claim 68, wherein said second storage device is configured to store at most a partial memory address of a redundant memory array of said memory device.

70. The system in claim 69, wherein said first storage device is configured to store a column address of said main memory array without a row address of said main memory array; and wherein said second storage device is configured to store a column address of said redundant memory array without a row address of said redundant memory array.

71. The system in claim 67, wherein said first storage device is configured to store at most a first partial memory address of a redundant memory array of said memory device; and wherein said second storage device is configured to store at most a second partial memory address of said redundant memory array.

72. The system in claim 71, wherein said redundant memory array comprises a plurality of redundant planes; and wherein said first partial memory address and said second partial memory address are incorporated into separate redundant planes.

73. Repair circuitry for a memory chip, comprising:

at least one redundant plane organized from memory cells of a redundant array on said chip; and

at least one register on said memory chip and configured to store data relevant to at least one redundant plane.

74. The circuitry in claim 73, wherein:

said at least one redundant plane comprises at least two redundant planes incorporating different memory cells from any one column of said redundant array; and

said at least one register comprises a register configured to store only a redundant column address of any one column of said redundant array.

75. The circuitry in claim 73, further comprising:

a redundant plane organized to incorporate at most a portion of any column of said redundant array; and

a register configured to store a redundant column address of any one column of said redundant array without storing any row address of said redundant array.

76. The circuitry of claim 73, wherein said at least one register comprises a register configured to store a redundant column address and further configured to exclude from storage a redundant row address; and wherein memory cells having said redundant column address are divided among at least two redundant planes.

77. Redundancy circuitry for a memory chip, comprising:

a redundant memory array on said memory chip and organized into at least one column; and

at least one register on said memory chip and configured to store a column address of said redundant memory array.

78. The circuitry in claim 77, wherein said redundant memory array is organized into a plurality of redundant planes; and wherein a totality of cells within each column of said plurality are divided among at least one group of redundant planes from said plurality.

79. The circuitry in claim 78, wherein said at least one register corresponds in number to said at least one group of redundant planes, and wherein each register of said at least one register is configured to store a column address of a column associated with a group of redundant planes.

80. A method of repairing a memory chip, comprising:

identifying a defective memory cell on said chip;

storing a column address of said defective memory cell in a first register on said chip;

identifying an available column of redundant memory cells on said chip;

storing a column address of said available column of redundant memory cells in a second register on said chip; and

replacing all memory cells sharing said column address of said defective memory cell with said available column of redundant memory cells.

81. The method in claim 80, wherein said act of replacing comprises:

accessing said available column of redundant memory cells using logic circuitry; and

using data from said second register as input to said logic circuitry.

82. The method in claim 81, further comprising clearing said second register.

83. The method in claim 82, further comprising:

clearing said first register;

identifying another defective memory cell on said chip;

storing a column address of said another defective memory cell in said first

register;

identifying another available column of redundant memory cells on said chip;

storing a column address of said another available column of redundant memory cells in said second register; and

replacing all memory cells sharing said column address of said another defective memory cell with said another available column of redundant memory cells.

84. A method of preparing to repair a memory array on a chip, said method comprising:

searching for all available columns of redundant elements; and

storing on said chip an address of an available column of redundant elements found during said act of searching.

85. The method in claim 84, wherein said storing act comprises storing an address of the first available column of redundant elements found during said act of searching.

86. The method in claim 85, wherein said act of storing an address of the first available column comprises storing an address of said first available column to the exclusion of storing any other available column of redundant elements found during said act of searching.

87. The method in claim 85, further comprising storing an address of another available column of redundant elements found during said act of searching.

88. The method in claim 87, further comprising storing an address of the last available column of redundant elements found during said act of searching.

89. The method in claim 88, wherein said act of storing an address of the last available column comprises:

storing said last available column in a register; and

clearing from said register any previously-stored address.

90. A method of storing data for a memory device, comprising:

providing a device on a semiconductor die, wherein said die incorporates said memory device; and

storing in said device data relating to a plurality of memory cells.

91. The method in claim 90, wherein said storing act comprises storing address data common to a plurality of memory cells.

92. The method in claim 91, wherein said storing act comprises refraining from storing address data that is uncommon to said plurality of memory cells.

93. The method in claim 92, wherein said storing act comprises storing a row address.

94. The method in claim 90, wherein said storing act comprises storing a column address.

95. The method in claim 94, wherein said storing act comprises storing a column address of a plurality of unused memory cells in a redundant array of said memory device.

96. The method in claim 94, wherein said storing act comprises storing a column address of a plurality of memory cells in a main array of said memory device, wherein at least one memory cell of said plurality has tested as being defective.